[Ho Chun Jian] **Approximate methods to reduce computational resources for on-board image formation**

SAR signal processing algorithms typically involves several transformation operations a on two-dimensional dataset, requiring extensive computational and memory resources. The goal of performing real-time processing of a SAR image with high swath-to-resolution ratio remains challenging despite improvements in embedded processing technology. This study approaches this problem through approximation and divide-and-conquer implementation.

By understanding the difference between ADC sampling rate and the FPGA clock rate, a divide and conquer approach is taken to split and stream the incoming data into multiple pipelines through a set of polyphase filters for concurrent processing. Doing so avoids the standard deskew processing which requires Fourier transform that can be costly to implement on FPGAs. The pipelined data is then processed using Polar Format Algorithm with an output centred convolution approach for interpolation, where the reduced data size in each pipeline is streamed from the range interpolation step to azimuth interpolation, avoiding buffering in memory and the need for in memory corner turn. For validation, a lab-based injection of SAR data was performed to demonstrate the processing.